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INTEGRATED CIRCUIT AND METHOD FOR INTERFACING TWO VOLTAGE DOMAINS USING A TRANSFORMER

Abstract

An integrated circuit designed to reduce on-chip noise coupling. In one embodiment, circuit (60) includes the following: a circuit transformer (62) capable of converting a noise sensitive input reference clock signal to an output signal having a voltage compatible with a predetermined sink voltage logic level; and a biased receiver network (64) having a PFET current mirror (74) coupled with a NFET current (72), the biased receiver transistor network designed to multiply the transformer signal to offset a mutual coupling loss of the transformer. In at least one alternative embodiment, the input reference clock signal originates at an off-chip clock generator circuit (42) and the output signal from receiver (64) is input to a PLL (44). In another alternative embodiment, the transformer is a monolithic integrated transformer. Another alternative embodiment of the present invention is a method of reducing on-chip noise coupling.